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Call for Participation  
Workshop on  
**SELSE 2, System Effects of Logic Soft Errors**

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University of Illinois at Urbana-Champaign, April 11-12, 2006

Soft error in logic is an emerging concern for advanced silicon technologies. SELSE 2 is intended to bring together a diverse group of participants from academia and industry to explore this problem from the device technology to systems behavior, simulation, and system level solutions. This will be a forum to discuss your most current research and opinions on the topic. We are interested in soliciting papers which cover the system level effects of logic SER from all perspectives. Papers addressing both future and current technologies are requested. Papers addressing error management in future technologies (including revolutionary nanotechnologies) will also be considered. Illustrative case studies as well as future scenarios are solicited.

Key questions to be addressed in the workshop presentations & discussions are:

- \* What are the “new” mitigation techniques?
- \* What is the overhead of soft error mitigation techniques?
- \* Can soft error mitigation techniques successfully handle other types of errors?
- \* How does one decide what mitigation technique is preferred?
- \* How is system level derating predicted and measured?
- \* What is the state of the art in system derating prediction?
- \* Would it be useful to develop standard terms and metrics?
- \* Can we develop a technology roadmap for SER?

Authors are requested to submit their extended abstracts for review to Wendy Bartlett (wendy.bartlett@hp.com) on or before January 30, 2006. Submissions should be PDF or Microsoft Word files that do not exceed 4 printed pages. Customary terms for copyright agreement and non-confidentiality will apply. Authors will be notified of paper outcome on February 20, 2006. The camera-ready formatted papers are due on March 20, 2006.

Registration information will be posted on the workshop website:

[www.selse.org](http://www.selse.org)

**Workshop Co-chairs**

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