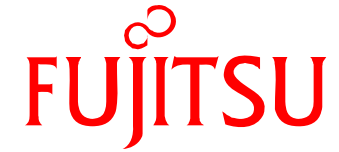


SELSE 2 Design Panel

H.Ando



- Processor Logic SER
 - 200K latches x 30% in-use x 0.001 fit =60fit
 - 8 Core CPU chip: MTBF ~200 years
 - Not a problem for low end servers (>100 years for 1~2 chips)
 - Marginal for high end servers (6 years for 32 chips)
 - Intolerable for Supercomputers (<1 day for 100,000 chips)
- Logic SER protection
 - Cost (chip area, power etc.) of protection vs. Cost of failure due to SER
 - System failure cost is high for life or death systems and large infrastructure systems
 - Method of protection
 - TMR is expensive in money and power
 - Detection and roll-back recovery: reasonable cost
 - This mechanism works for other source of errors
 - Major obstacle of implementation is designers' mindset and skills

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