

# Single-Event-Upset Critical Charge Measurements and Modeling of 65nm Silicon-on-Insulator Latches and Memory Cells

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## Abstract

Experimental and modeling results are presented on the critical charge required to upset exploratory 65nm silicon-on-insulator (SOI) circuits. Using a mono-energetic, collimated, beam of particles the charge deposition was effectively modulated and modeled.

## I. Introduction

Radiation induced Single Event Upsets (SEU) in logic and memory circuits continue to be a key issue for advanced CMOS technologies (1). For high performance 65nm circuits, the critical charge required to upset the circuit can be very small. The 65nm latch and memory circuits can be upset by a wide range of ionizing particles striking the device at many angles. Accurately modeling these upsets is necessary for determining the appropriate device parameters to obtain both high circuit performance and high reliability.

This paper presents an experimental and modeling study of the critical charge necessary to upset 65nm silicon-on-insulator (SOI) circuits. The experimental data is obtained using a mono-energetic beam of light particles (alpha, lithium) from a Tandem accelerator. Using the beam at specific energies and angles provides an effective method to control the amount of charge that is deposited in the circuit. With this technique, the critical charge can be accurately determined.

Modeling 65nm SOI latches and memory circuits for radiation effects is very complex. The methodology used for SPICE simulations and the device parameters used in a SPICE model can make significant differences in the results. SPICE modeling of these devices is discussed in Reference (2). The modeling discussed in this paper has been done with the Fielday (3, 4) model. Fielday can be directly compared to the experimental results including charge deposition, angle and location of the striking particle.

## II. Experimental setup

The IBM T.J. Watson Research Center has a 3MV Tandem Van de Graaff accelerator that is used for SEU experiments. Inside the SEU exposure vacuum chamber the wire bonded chip is positioned on a goniometer so that its position and rotational orientation can be adjusted with respect to the beam. A silicon (Si) surface-barrier detector was periodically positioned upstream with respect to the chip and was used for monitoring the particle flux. The average flux was typically  $5E6$  ions/cm<sup>2</sup>-s. The beam flux was measured before and after each chip exposure. The beam was defocused at the plane of the chip. The photograph in Figure 1 shows the aperture / surface-barrier detector in front, as well as the chip, rotated with respect to the beam.

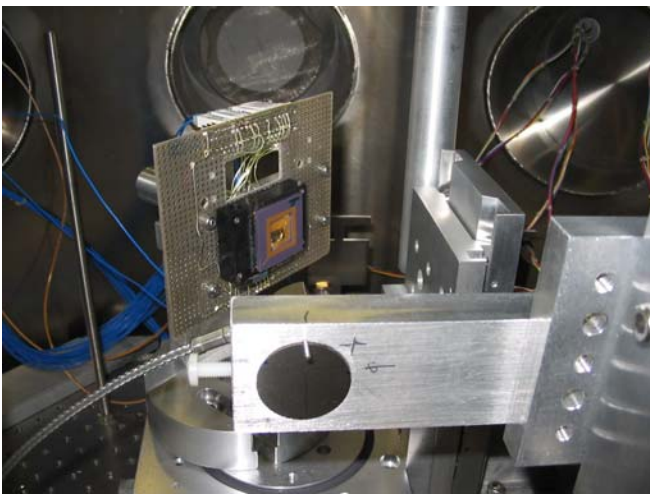


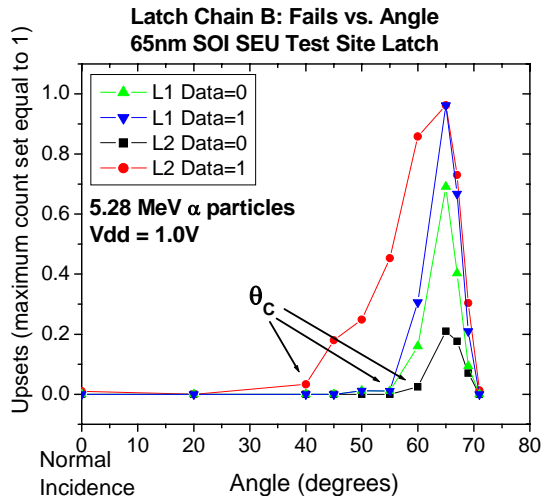
Fig. 1. Chip Test Site mounted in SEU vacuum chamber.

SRAM or latch chips were initialized with a known test pattern and then exposed for various periods of time ranging from 10 to 30s. Subsequently, the data in the chip was read and any changes in the initial stored pattern, e.g., from 0 to 1 or from 1 to 0, were recorded. This procedure was repeated for each angle with the beam flux monitored both before and after each exposure. The surface linear energy transfer (LET) was calculated through the back end of the line (BEOL) using the measured chip BEOL thickness, an estimated volume fraction of Cu and insulator and their respective stopping powers.

### III. Experimental data and analysis

Using IBM's 65nm SOI technology (5), a series of test sites were built with exploratory array cells (SRAM) and latch designs to study the critical charge needed to upset these circuits. The array data was taken on only one of the 1Mb array cell designs. More extensive testing was done on the latch designs. Latch data were taken on 16 different latch designs in both the data=0 and data=1 state. Some of the latch designs were specifically modified to make the circuits very sensitive to alpha particles. The 16 latch designs were built on 8 different scan chains containing both an L1 and L2 latch. Most of these chains consisted of 12,000 L1/L2 latch pairs. Data were typically taken at several voltages ranging from 0.8 - 1.2V and several different energies were used for the incident particles. The test sites were built using only a limited number of wiring levels with a total BEOL thickness of 9.5 microns.

Figure 2 is an example of the data obtained on one of the scan chains and shows the fail rate as a function of angle for both data states of the L1 and L2 latches using 5.28 MeV alpha particles. The alpha particle energy was chosen to allow for the maximum stopping power of the alpha particle to strike the active region of the device over the range of angles used in the experiment. The fail data shown in Fig. 2 has been normalized, with the maximum fail count set equal to 1, since the absolute fail rate is not required to obtain the critical charge of the latch. From the data vs. angle results, it is possible to determine a critical angle ( $\theta_c$ ) at which fails are first observed. Using a Monte-Carlo analysis of the stopping power of the incident particles, the critical angle can be converted into the critical charge deposited in the device.



Vdd = 1 V	Latch Chain A	Latch Chain B
L1 Data = 0	$\theta_c = 20^\circ$ Qcrit = 0.5 fC	$\theta_c = 55^\circ$ Qcrit = 0.9 fC
L1 Data = 1	$\theta_c = 55^\circ$ Qcrit = 0.9 fC	$\theta_c = 55^\circ$ Qcrit = 0.9 fC
L2 Data = 0	$\theta_c = 50^\circ$ Qcrit = 0.8 fC	$\theta_c = 60^\circ$ Qcrit = 1.0 fC
L2 Data = 1	$\theta_c = 45^\circ$ Qcrit = 0.7 fC	$\theta_c = 40^\circ$ Qcrit = 0.6 fC

Fig. 2. Latch Chain B: SEU vs. angle

Table 1. Critical charge of latches A & B

Shown in Table 1 is the critical charge angle and critical charge data that has been obtained for two of the latch chains, A & B. Latch Chain B data vs. angle is also shown in Fig. 2. Additional

data will be shown in the full paper. As seen in Table 1, the critical charge for these latches was determined to be approximately 0.5 – 1.0 fC for both the data=0 and data=1 state. This small value of the critical charge can be easily obtained by a wide range of alpha particle energies, angles, and hit locations on these latches.

#### IV. Fielday Modeling

Device modeling of single events in small circuits was performed using the mixed-mode capability of Fielday (3,4). The L1 latch, as described above, (Chain A) was defined and simulated. The circuit is shown in Figure 3. Device structures were defined using process simulations calibrated to hardware. For most simulations, 2D devices were used and scaled by the device width. The DC operating point of the circuit was first calculated assuming either the data 0 or data 1 state. A transient analysis was then performed of a radiation event in either of the “OFF” devices N53 or P54 for the data 0 state, or devices N59 or P49 for the data 1 state. The radiation event was modeled using an  $\alpha$ -particle induced charge generation model, calibrated to the data shown in (6). Typically, simulations such as this require approximately 12-24 cpu-hours to complete on recent vintage AIX workstations.

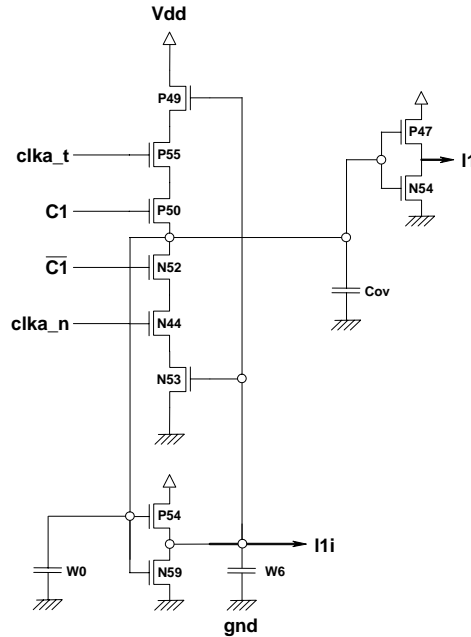


Fig. 3. L1 Latch (Chain A) simulated with Fielday.

The critical charge is determined by assuming that the  $\alpha$ -particle strikes at normal incidence through the center of the channel. The charge generation model has an adjustable parameter to scale the ionization. A simple binary hunt algorithm is implemented to submit simulation jobs in parallel with different charge scaling factors. Iterations on this scaling factor are performed to determine the charge generation that just causes the logic state to switch. Results of this calculation for the L1 Latch (Chain A) are shown in Table 2.

Device	Data 0 (fC)	Data 1 (fC)
NFET	0.53	0.98
PFET	1.50	>10.0

Table 2. Critical charge for an L1 Latch (variant A) at Vdd=1V calculated using Fielday.

Simulation results compare favorably with the measured hardware. Using these results, the relative contribution of NFET and PFET strikes to the soft error rate can be quantified using the SEU simulator SEMM2 (7). These simulation results were further used to help develop a Qcrit model using SPICE through a detailed comparison of the time evolution of the device contact voltages and internal potentials, as described in (2). Additional single event simulation studies undertaken were the effects of non-normal incidence strikes including rotation angle, investigation of technology variants, Qcrit in SRAM cells and Qcrit fluctuations due to process variations.

## V. Conclusions

An extensive experimental and modeling study has been completed on special test-site latch designs and SRAM cells built in the 65 nm SOI technology. The circuits were irradiated with alpha beams of various energies delivered by the Yorktown Tandem accelerator. The fail rate was mapped as a function of incident angle. By using a Monte Carlo model, the energy loss was correlated to the critical charge needed to upset the circuit. The SRAM and latch circuits were modeled with the Fielday program. The critical charge determined by these simulations closely matched the experimental results.

The key result of this work is that both SRAM and test-site latch designs built in 65 nm SOI technology can be very sensitive to alpha particles. Many variations of latch designs were tested showing a wide range of critical charge values and sensitivities to alpha particles. With the increasing sensitivity to alpha particles, choosing latch designs consistent with the overall soft error rate for the system will be important.

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