



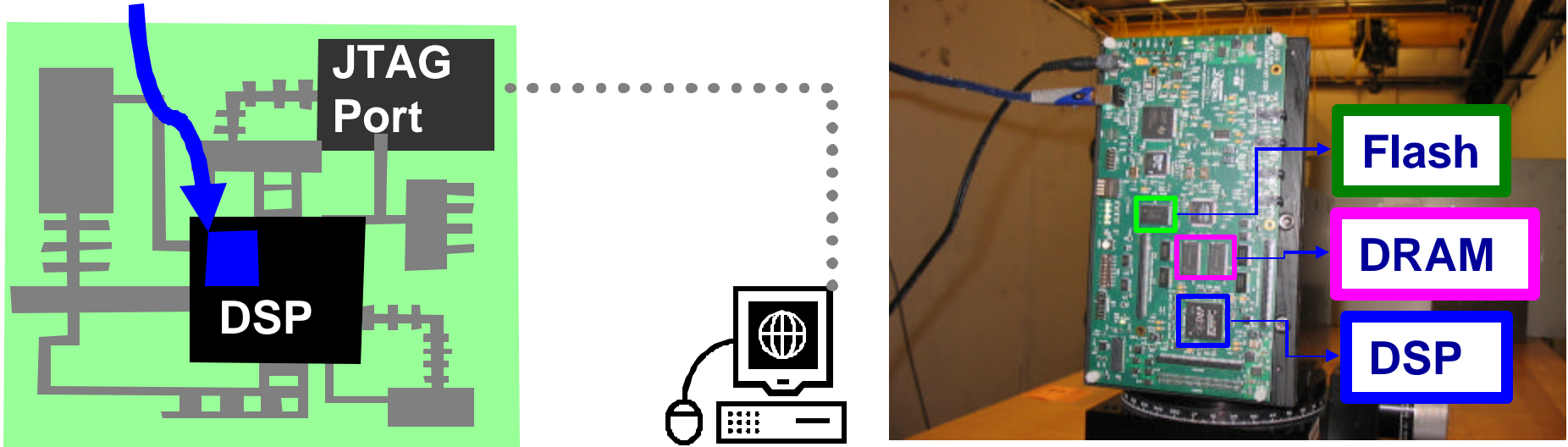
MEMORY FAILURE SIGNATURES OF LOGIC OR SYSTEM SOFT ERROR

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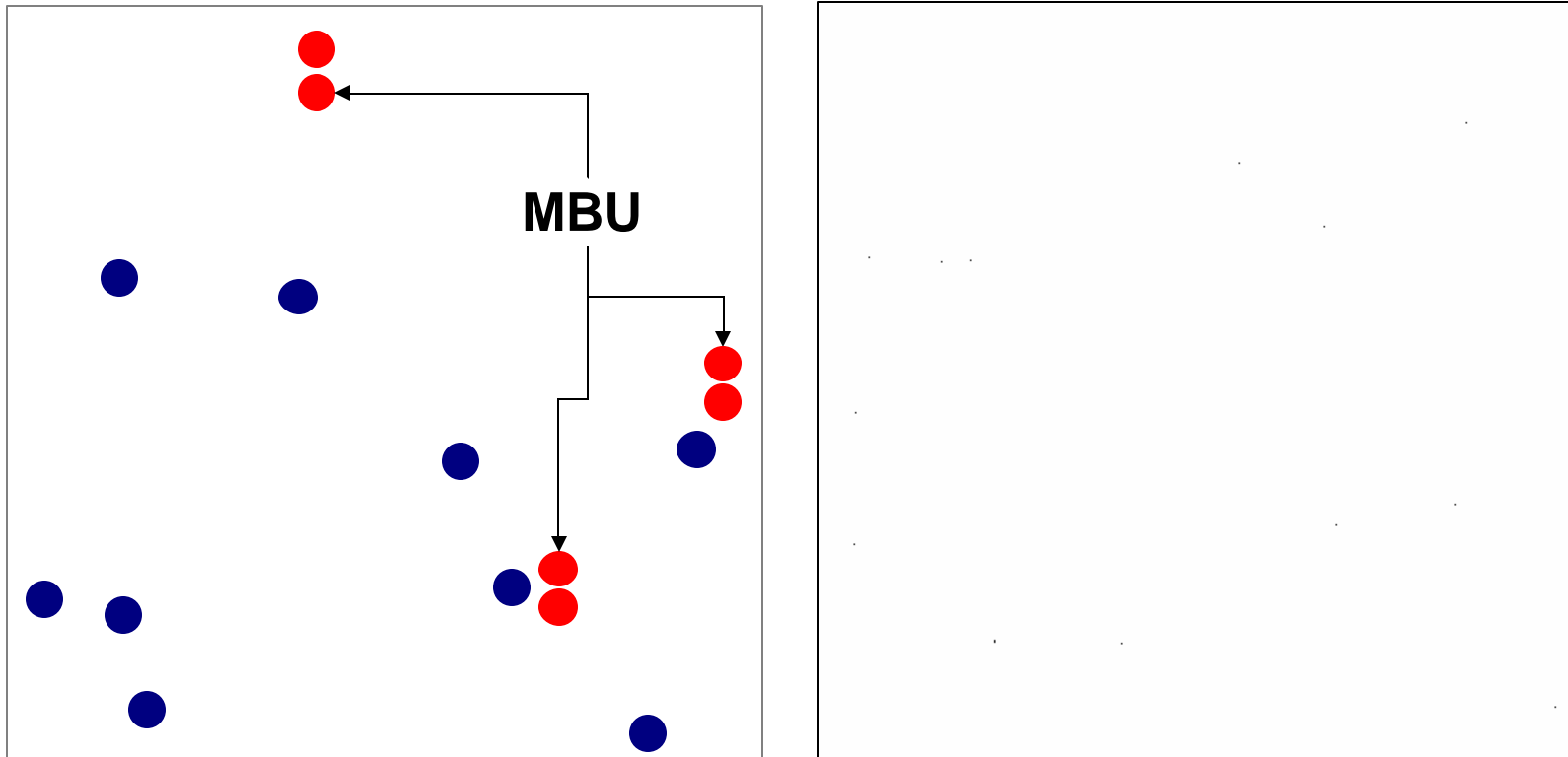
Experimental Setup

Testing Program



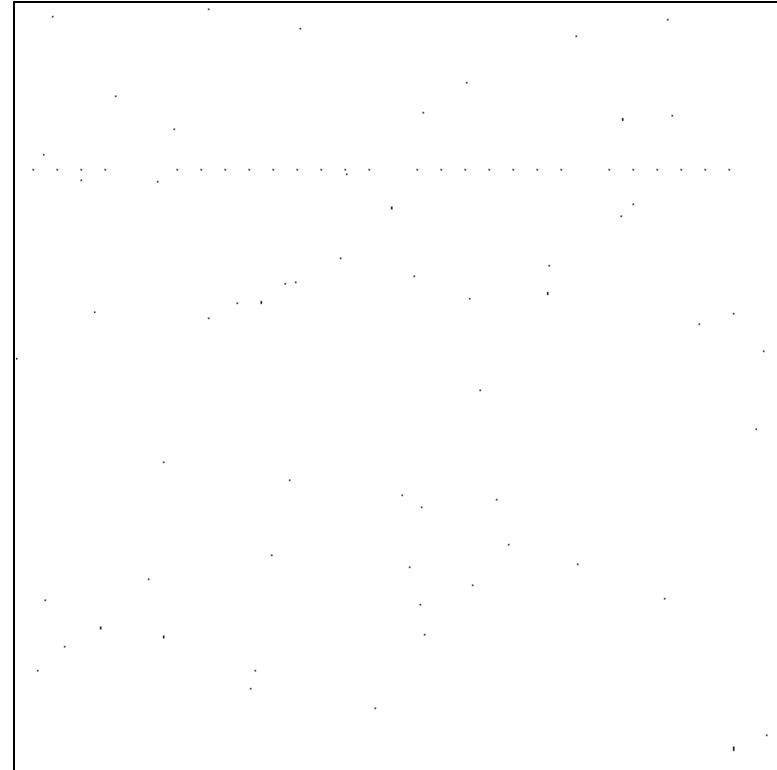
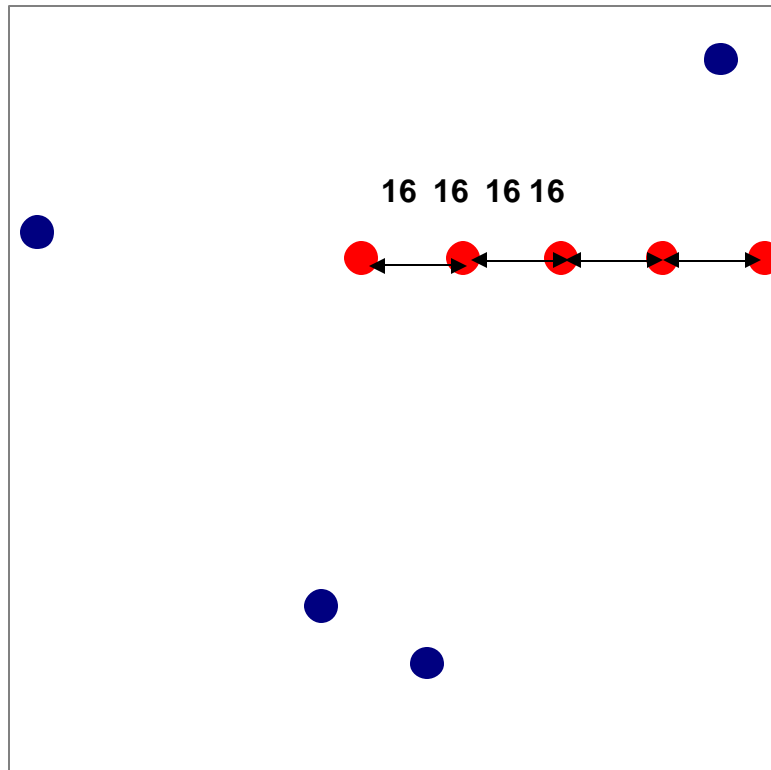
- Testing program transfer to DUT through JTAG
- Write known pattern into memory
- Continuously reading the memory content to the PC

SBU & MBU



- **Single bit upset is distributed randomly**
- **Multiple bit upsets are two or more adjacent bit failing caused by one particle**

False Write



- **Failing bits are on the same row and it occurs every 16 bits indicates a false write**

System Reset

(a) Sample memory snip after reset

1	0	1	0	1	1	1	0
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1	1	1	0	1	0	1	1
---	---	---	---	---	---	---	---

(b) Before neutron exposure

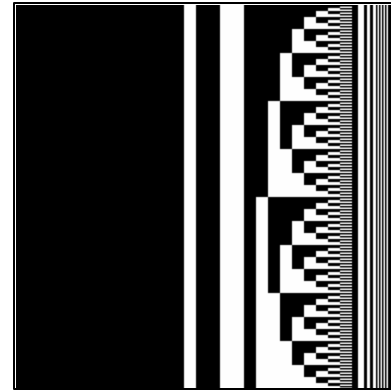
0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---

0	0	0	0	0	0	0	0
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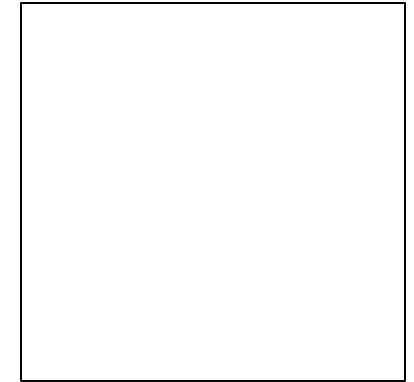
(c) After neutron exposure

1	0	1	0	1	1	1	0
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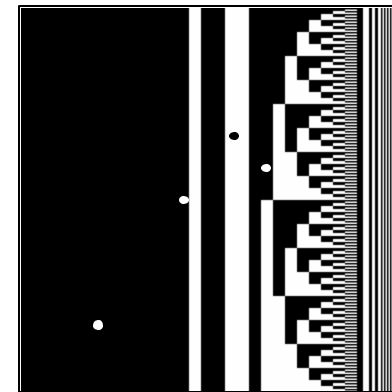
1	1	1	0	1	0	1	1
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(a)



(b)



(c)

- The memory content shows great resemblance of reset data pattern

Failure Signature Summary

- **Single Bit Upset** and **Multiple Bit Upset** can be detected by analysis of physical memory map
- Logic failure might cause **False Write** in memory content
- **System Reset** may lead to abnormally high SER number during that test run
- Logic or System failure can cause SER outliers in memory SER testing